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UTILITY PATENT APPLICATION TRANSMITTAL
(Large Entity)

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Docket No.
FI996085

Total Pages in this Submission
3

TO THE ASSISTANT COMMISSIONER FOR PATENTS
Box Patent Application
Washington, D.C. 20231

Transmitted herewith for filing under 35 U.S.C. 111(a) and 37 C.F.R. 1.53(b) is a new utility patent application for an invention entitled:

CIRCUIT AND METHODS TO IMPROVE THE OPERATION OF SOI DEVICES

and invented by:

1) Roy Childs Flaker (deceased), 2) Louis L. Hsu, 3) Jente B. Kuang

If a CONTINUATION APPLICATION, check appropriate box and supply the requisite information:

☐ Continuation ☒ Divisional ☐ Continuation-in-part (CIP) of prior application no. 09/063,823

Which is a:

☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application no._____

Which is a:

☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application no._____

Enclosed are:

Application Elements

1. ☒ Filing fee as calculated and transmitted as described below
2. ☒ Specification having 20 pages and including the following:
   a. ☒ Descriptive Title of the Invention
   b. ☒ Cross References to Related Applications (if applicable)
   c. ☐ Statement Regarding Federally-sponsored Research/Development (if applicable)
   d. ☐ Reference to Microfiche Appendix (if applicable)
   e. ☒ Background of the Invention
   f. ☒ Brief Summary of the Invention
   g ☒ Brief Description of the Drawings (if applicable)
   h. ☒ Detailed Description
   i. ☒ Claim(s) as Classified Below
   j. ☒ Abstract of the Disclosure

Application Elements (Continued)

UTILITY PATENT APPLICATION TRANSMITTAL (Large Entity) *(Only for new nonprovisional applications under 37 CFR 1.53(b))*	Docket No. FI996085
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3. ☒ Drawing(s) (when necessary as prescribed by 35 USC 113) 6 sheets

a. ☒ Formal Number of Sheets: 6
b. ☐ Informal Number of Sheets: ___

4. ☒ Oath or Declaration

a. ☐ Newly executed (original or copy) ☐ Unexecuted

b. ☒ Copy from a prior application (37 CFR 1.63(d)) (for continuation/divisional application only)

c. ☒ With Power of Attorney ☐ Without Power of Attorney

d. ☐ DELETION OF INVENTOR(S)
Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. 1.63(d)(2) and 1.33(b).

5. ☐ Incorporation By Reference (usable if Box 4b is checked)
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. ☐ Computer Program in Microfiche (Appendix)

7. ☐ Nucleotide and/or Amino Acid Sequence Submission (if applicable, all must be included)
a. ☐ Paper Copy
b. ☐ Computer Readable Copy (identical to computer copy)
c. ☐ Statement Verifying identical Paper and computer Readable Copy

Accompanying Application Parts

8. ☐ Assignment Papers (cover sheet and document(s))

9. ☐ 37 CFR 3.73(B) Statement (when there is an assignee)

10. ☐ English Translation Document (if applicable)

11. ☐ 37 CFR 3.73(B) Statement (when there is an assignee)

12. ☒ Preliminary Amendment

13. ☒ Acknowledgement postcard

14. Certificate of Mailing
☐ First Class ☐ Express Mail (Specify Label No.):

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Accompanying Application Parts (Continued)

15. ☐ Certified Copy of Priority Document(s) (if foreign priority is claimed)

16. ☐ Additional Enclosures (please identify below):

Information Disclosure Statement, Forms PTO-1449 & PTO-892

Fee Calculation and Transmittal

CLAIMS AS FILED

For	#Filed	#Allowed	#Extra	Rate	Fee
Total Claims	8	- 20 =	9	x $18.00	$0.00
Indep Claims	1	- 3 =	0	x $0.00	$0.00
Multiple Dependent Claims (check if applicable) ☐					$0.00
				BASIC FEE	$690.00
OTHER FEE (specify purpose)					$0.00
				TOTAL FILING FEE	$690.00

☐ A check in the amount of to cover the filing fee is enclosed.
☒ The Commissioner is hereby authorized to charge and credit IBM Corporation Deposit Account No. 09-0458 as described below. A duplicate copy of this sheet is enclosed.

☒ Charge the amount of **$690.00** as filing fee.
☒ Credit any overpayment.
☒ Charge any additional filing fees required under 37 C.F.R. 1.16 and 1.17.
☐ Charge the issue fee set in 37 C.F.R. 1.18 at the mailing of the Notice of Allowance, pursuant to 37 C.F.R. 1.311(b).

Date: 6-7-00

Eric J. Franklin, Reg. No. 37,134 (Signature)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	:	
ROY CHILDS FLAKER (deceased)	:	Attorney Docket: FI996085
Serial No.: Con't of 09/063,823	:	Art Unit: to be assigned
Filed: herewith	:	Examiner: to be assigned

For: CIRCUITS AND METHODS TO IMPROVE THE OPERATION OF SOI DEVICES

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, DC 20231

Sir:

Prior to examination, please amend the above-identified application as follows:

In the Specification:

Page 1, line 1, after the title, please insert:

--This application is a continuation of U.S. patent application serial number 09/063,823, filed April 22, 1998, which claims priority from U.S. provisional patent application serial number 60/044,251 filed on April 23, 1997.--.

In the Claims:

Please cancel claims 1-5 without prejudice to their reentry.

Remarks:

Claims 6-13 are now pending in this case. Applicants have canceled claims 1-5, which were prosecuted in the parent application.

In the event that the Examiner believes that an interview would serve to facilitate the prosecution of this application, Applicants respectfully urge the Examiner to contact the undersigned at the telephone number listed below.

The undersigned hereby authorizes the Commissioner to charge any insufficient fees or credit any overpayment associated with this communication to deposit account no. 22-0185.

Respectfully submitted,

Date: 6-7-00

Eric J. Franklin, Reg. No. 37,134
Attorney for Applicants
Pollock, Vande Sande & Amernick
1990 M Street, N.W.
Washington, DC 20036-3425
Telephone: 202-331-7111
Facsimile: 202-293-6229

CIRCUIT AND METHODS TO IMPROVE THE OPERATION OF SOI DEVICES

BACKGROUND OF THE INVENTION

1. Technical Field

This invention generally relates to integrated circuits. More specifically, the present invention relates to enhancing the performance of Silicon On Insulator (SOI) devices.

2. Background Art

Today, our society is heavily dependent on high-tech electronic devices for everyday activity. Integrated circuits are the components that give life to our electronic devices. Integrated circuits are found in widespread use throughout our country, in appliances, in televisions and personal computers, and even in automobiles. Additionally, manufacturing and production facilities are becoming increasingly dependant on the use of integrated circuits for operational and production efficiencies. Indeed, in many ways, our everyday life could not function as it does without integrated circuits. These integrated circuits are manufactured in huge quantities in our country and abroad. Improved integrated circuit manufacturing processes have led to drastic price reductions for these devices.

The traditional integrated circuits fabrication process is a series of steps by which a geometric pattern or set of geometric patterns is transformed into an

operating integrated circuit. An integrated circuit consists of superimposed layers of conducting, insulating, and transistor-forming materials. By arranging predetermined geometric shapes in each of these layers, an integrated circuit that performs the desired function may be constructed. The overall fabrication process typically consists of the patterning of a particular sequence of successive layers using various chemicals as etchants. Many different processes exist for creating a pattern on the silicon wafer, with different processes being specifically adapted to produce the desired type of integrated circuit.

One relatively new process for fabricating integrated circuit devices is commonly known as Silicon On Insulator (SOI). SOI devices are semiconductor devices which are formed within a thin silicon layer that overlies an electrically insulating region formed over an integrated circuit substrate material. This insulating region may include, for example, a layer of SiO_2 deposited over a semiconductor substrate material such as silicon or gallium arsenide. This fabrication process allows devices to be created which are electrically isolated from the substrate. SOI devices offer several advantages over conventional semiconductor devices.

For example, SOI devices typically have lower parasitic capacitances which, in turn, translate into faster switching times for the resulting circuits. In addition, the well-known but undesirable phenomenon of "latchup," which is often exhibited by conventional Complementary Metal-Oxide Semiconductor (CMOS) devices, is avoided when CMOS devices are manufactured using SOI fabrication processes. SOI devices are also less susceptible to the adverse effects of ionizing radiation and, therefore, tend to be more reliable in

applications where ionizing radiation may shorten the life of traditional integrated circuits.

The advantageous characteristics of SOI devices result from the dielectric isolation described above. While providing many advantages, this dielectric isolation also produces some difficulties not encountered with more conventional integrated circuit devices. In conventional devices, electrical interactions occur between the device substrate and the device active region, e.g. the current-carrying portion of the device, such as the current channel of a Metal-Oxide Semiconductor Field Effect Transistor (MOSFET). Occasionally, accumulated charge in the device active region can alter the device threshold voltage V_T (i.e., the voltage at which the current channel of an enhancement-mode MOSFET begins to conduct current). However, in conventional devices, this accumulated charge is readily removed through the substrate by applying an appropriate voltage to the substrate which attracts the accumulated charge away from the active layer, into the substrate, and out through a conductive lead. For example, a negative voltage applied to the substrate attracts holes from the active layer into the substrate, while a positive voltage attracts electrons. Alternatively, it is possible to change the threshold voltage of a conventional integrated circuit device, if desired, by applying a voltage to the active region through the electrically connected substrate. This is known as the "body effect."

In contrast, in a typical SOI device, the insulating region prevents both the conduction of charge from the active region into the substrate, and the application of a voltage to the active region through the substrate. Thus, the lack of flexibility in the operation of an integrated circuit device due to the SOI insulating region is often inconvenient. For example, during operation of a

typical SOI MOSFET, electrical charge can accumulate in the body of the device, (the region of the MOSFET between the source and the drain), until the concomitant electrical potential increases sufficiently to produce a shift in the threshold voltage (V_T) of the device. This shift can adversely affect the operation of the circuit and introduce errors into the information being processed by the device. The charge accumulates on the body of the SOI transistors in a circuit whenever the circuit is not being supplied with voltage.

For example, in a typical circuit using bulk CMOS devices, the body of an n-FET device will be connected to ground and the body of a p-FET device will be connected to the supply voltage (V_{DD}). Therefore, even when no voltage is applied to the n-FET or the p-FET, the body potential is controlled by the connection to either ground or V_{DD} and the operational V_T will be in keeping with standard design parameters for each device. In contrast, the body of an SOI device is not connected to either ground or V_{DD} and, therefore, the body of the device can "float" to any voltage level. In addition, thermal fluctuations can also cause electrical charges to accumulate in the body of the transistors. Over a period of time, this charge can accumulate and can cause V_T to be lower than the specified design parameters and the transistor will switch on before it should. If V_T has been altered significantly, the operation of the circuit can be effected. For example, in synchronization circuits with critical timing requirements, the transistor may not switch on at the appropriate time and the circuit may not operate at all.

One specific example of the problems associated with SOI integrated devices is illustrated in FIG. 4. In FIG. 4, a typical memory circuit 400 with 256 local word line drivers comprises a highest order local word line

(LWL255) circuit 430 which includes transistor 432 and node 431; a lowest order local word line circuit (LWL0) 440; a segment driver 450 which includes a pass transistor 451; and a select line 460. The illustrated circuit represents a small portion (one segment) of a much larger memory array on a typical memory chip. The lowest order local word line (LWL0) circuit 440 is driven by a low order Global Word Line (GLW0). The highest order local word line (LWL255) circuit 430 is, correspondingly, driven by a high order Global Word Line 255 (GWL255). The intervening word lines (not shown) are likewise driven by other global word lines (not shown).

The individual segments in a memory array are accessed by activating segment driver 450. When memory circuit 400 is not being accessed, all of the global word lines are deselected and are at a low voltage level and, due to the operation of the transistors connected to GWL255 shown in circuit 430, node 431 is connected to V_{DD}. All of the remaining word lines circuits (GWL0-GWL254) operate in the same way. When segment driver 450 is not selected, transistor 432, and the corresponding transistors in the other local word driver circuits, are not driven and are therefore turned off. Circuit 435 represents the load of the remaining word line drivers. Due to the accumulated charge stored on each of the transistors represented by this load, select line 460 appears to circuit 400 as if it were a large capacitor with a stored charge.

When segment driver 450 is activated, one of the active global word lines will provide access to a local word line for reading or writing to a specific memory location. This process is accomplished as follows. The memory chip is activated by supplying a signal to the CLOCK input of segment driver 450. The control (CTL) or segment signal is used to select one of the memory

subarrays or segments for reading or writing. After a small propagation delay, the control circuit (not shown) creates a decoding signal DECODE that activates the appropriate subarray by driving select line 460 to low. When all three of the input signals to segment driver 450 are active, node 431 in the local word line driver circuit 430 is discharged through select line 460 and pull-down transistor 451 in segment driver 450.

At this point, although only one of the 256 global word lines is selected, segment driver 450 must discharge all of the accumulated charge in the body of each transistor corresponding to transistor 432 in local word line driver 430 for each of the 256 local word line drivers. This is known as "fan-out" loading. As described earlier, the bodies of the SOI transistors have a tendency to accumulate electrical charge. When a given memory segment is not being accessed for a period of time (i.e. 0.1ms for a typical n-FET device) , an electrical charge can accumulate in the body of each one of the SOI transistors. Then, when the memory segment is first accessed, the charge on each of the transistors corresponding to transistor 432 must be discharged. The "first access" is considered to be when the segment is first used to read or write data after a period of inactivity. If subsequent accesses are to the same memory segment, no charge sufficient to cause delays will have been accumulated. If, however, a different memory segment is subsequently accessed, the previously accessed memory segment may, once again, need to be discharged prior to subsequent accesses. Memory access is delayed until the electrical charge is dissipated.

The fan-out loading effect is known for a tendency to slow down memory access times associated with SOI devices, especially during the first cycle of

operation, when the accumulated charge on the body of the transistors is the greatest. Also, the greater the physical distance between segment driver 450 and the selected local word line driver, the harder it is to drive. Due to the propagation delay inherent in the physical circuit wiring, body charges in more distant devices take longer to discharge through the long, relatively resistive wire. However, after the first access cycle, the SOI loading effect is diminished significantly. This is because, once the accumulated body charges in all of the N-channel FET pull-down devices have been discharged, a relatively long period of time is needed to build up the charge on the body of the transistors again. Therefore, as long as the memory access requests are to the same subarray or segment, there will be no additional access delay associated with discharge propagation delays. By logical extension, the worst access times for an SOI memory device is generally the first access cycle for a device that is located the farthest distance from segment driver 450.

The loading effect described above can be completely eliminated by connecting the body of an SOI device to a reference ground. Referring now to FIG. 7, a SOI transistor 700 formed with a body contact for connecting the body of transistor 700 to ground is shown. SOI transistor 700 has a body implant mask region 710, a source/drain implant mask region 720, a T-shaped gate 725; a source contact 730, a drain contact 740, and a body contact 750. Body contact 750 is typically connected to ground for an n-channel device and to V_{DD} for a p-channel device. The creation of body contact 750 requires additional processing and mask steps when transistor 700 is being fabricated. If body contact 750 is connected to ground, the problems associated with charge build-up on the body of transistor 700 are eliminated. However, this will also negatively impact circuit operation in at least two ways. First, circuit overhead (i.e. the amount of

area needed to fabricate the circuit) is significantly increased and, second, the speed advantage inherent in SOI circuits is also eliminated, because the lower variable V_T of SOI devices is not longer present.

Therefore, there exists a need to provide a way to take advantage of the benefits of SOI device characteristics without suffering the possible negative implications of SOI fabricated devices. In addition, the methods employed should not unnecessarily diminish or destroy the positive advantages provided by implementing circuits and devices using SOI technology.

DISCLOSURE OF INVENTION

According to the present invention, a circuit and methods for enhancing the operation of SOI fabricated devices are disclosed. In a preferred embodiment of the present invention, a pulse discharge circuit is provided. Here, a circuit is designed to do a pulse discharge that will eliminate the accumulated electrical charge on the SOI devices in the memory subarray just prior to the first access cycle. As explained above, once the accumulated charge has been dissipated, the speed penalty for successive accesses to the memory subarray is eliminated or greatly reduced. With a proper control signal, timing and sizing, this can be a very effective method to solve the problem associated with the SOI loading effect.

Alternatively, instead of connecting the bodies of all SOI devices in a memory circuit to ground, the bodies of the speed-critical devices are selectively connected to a reference ground. This would enable the circuit to retain most of the speed advantages associated with SOI devices while overcoming the loading

problem described above. With this preferred embodiment of the present invention, the major delay caused by the bipolar loading effect is minimized while the speed advantage due to providing a low Vt effect is preserved. The overall body resistance of the individual devices has a minimal effect on the device body potential.

The foregoing and other features and advantages of the invention will be apparent from the following more particular description of preferred embodiments of the invention, as illustrated in the accompanying drawings.

BRIEF DESCRIPTION OF DRAWINGS

The preferred embodiments of the present invention will hereinafter be described in conjunction with the appended drawings, where like designations denote like elements, and:

FIG. 1 is a perspective view of a portion of a bulk CMOS wafer:

FIG. 2 is a perspective view of a portion of an SOI wafer;

FIG. 3 is a block diagram of a circuit according to a preferred embodiment of the present invention;

FIG. 4 is a schematic of a local word line driver array for a typical memory circuit;

FIG. 5 is a block diagram of the circuit of FIG. 4 including a dynamic pulse discharge circuit according to a preferred embodiment of the present invention;

FIG. 6 is a schematic of the circuit of FIG. 5 including a dynamic pulse discharge circuit according to a preferred embodiment of the present invention; and

FIG. 7 is a plan view of an SOI transistor fabricated with a body contact.

BEST MODE FOR CARRYING OUT THE INVENTION

The present invention relates to the use and operation of integrated circuit transistors, particularly SOI transistors. For those individuals who are not familiar with CMOS and SOI fabricated devices, the Overview section below presents some basic concepts that will help to understand the invention. Those who are skilled in the art may wish to skip this section and begin with the Detailed Description Section instead.

OVERVIEW

Referring now to FIG. 1, a portion of a typical bulk CMOS wafer 100 includes: a substrate 110; an n-well 120; an n-well contact 125; a p-well 130; n^+ source and drain diffusions 135; polysilicon gate contacts 140; p^- source and drain diffusions 145; a p-well contact 155; a surface isolation 160; an n-channel 170; an n-body 175; a p-channel 180; a p-body 185, and a gate oxide 190.

The designation of a particular device as a p-channel device or an n-channel device depends on the type of fabrication process used to create the device. Substrate 110 is any semiconductor material known to those skilled in the art. The various wells and contacts are created by using different types of constituents when the wafer is being fabricated. In normal operation, n-well contact 125 is connected to V_{DD} and p-well contact 155 is connected to ground.

Referring now to FIG. 2, a portion of a typical SOI wafer 200 includes: a substrate 210; polysilicon gate contacts 140; a buried oxide layer 220; and an active region 230. Active region 230 is a thin layer of silicon and includes n^- source and drain diffusions 135; p^- source and drain diffusions 145; a surface isolation 160; an n-channel 170; a n-body 175; a p-channel 180; a p-body 185, and gate oxide 190.

Substrate 210 is any semiconductor material, or metal, or glass, known to those skilled in the art. Source and drain diffusions 135 and 145 will typically abut buried oxide layer 220. Surface isolation 160 and buried oxide layer 220 serve to electrically isolate source and drain diffusions 135 and 145, preventing electrical charge from being transferred to and from the devices through substrate 210.

DETAILED DESCRIPTION

Referring now to FIG. 3, a circuit 300 in accordance with a preferred embodiment of the present invention comprises: a pulse body discharge circuit 310; a circuit A 320; a circuit B 330; a control signal 340; an operation signal 350; a transistor 360; a reference ground 370; and a discharge path 380. Circuit 320 and circuit 330 may be any type of analog or digital logic device or circuit, including nand gates, memory circuits, microprocessors, and microcontroller circuits. Other examples of circuits 320 and 330 include voltage regulators, clock generation circuits, etc. In operation, transistor 360 acts as a switch for interconnecting circuits 320 and 330 whenever operation signal 350 is activated. Operation signal 350 is generated by a control circuit (not shown). Pulse body discharge circuit 310 can be used to enhance the switching speed of transistor 360. Just prior to activating operation signal 350, control signal 340 is

activated. Control signal 340 is also activated by the control circuit. When control signal 340 is activated, pulse body discharge circuit 310 provides a path from transistor 360 to reference ground 370 via discharge path 380. Therefore, before transistor 360 is activated by operation signal 350, the body of transistor 360 is completely discharged.

Referring now to FIG. 5, a memory circuit 500 in accordance with a preferred embodiment of the present invention includes: a pulse generator 510 that is a part of a dynamic pulse discharge circuit 310; local word line drivers 430 and 440; a segment driver 450; a select line 460; and the various signals explained in conjunction with FIG. 4 above. This figure illustrates how the circuit of FIG. 3 can be adapted for use in a computer memory application to provide faster switching times for memory circuit 500. Pulse generator 510 provides the discharge pulse that discharges the bodies of the SOI devices in memory circuit 500. Dynamic pulse discharge circuit 310 and pulse generator 510 are described in greater detail below.

Referring now to FIG. 6, memory circuit 500 of FIG. 5 is shown in schematic form. The components shown in memory circuit 500 are the same as in FIG. 5. Memory circuit 500 with 256 local word line drivers includes: a highest order local word line (LWL255) circuit 430; a lowest order local word line circuit 440; a segment driver 450; and a select line 460. As before, memory circuit 500 represents a small portion (one segment) of a much larger memory array on a typical memory chip. Lowest order local word line (LWL0) circuit 440 is driven by a low order Global Word Line (GLW0). Highest order local word line (LWL255) circuit 430 is, correspondingly, driven by a high order Global Word Line 255 (GWL255). The intervening word lines (not shown) are likewise driven by other global word lines (not shown). The

individual segments in a memory array are accessed by activating segment driver 450.

When segment driver 450 is activated, the active global word line will provide access to a local word line for reading or writing to a specific memory location. This process is accomplished as follows. The memory chip is activated by supplying a signal to the CLOCK input of segment driver 450. The control (CTL) or segment signal is used to select one of the memory subarrays or segments for reading or writing. In circuit 500, CTL is also supplied as an input signal to pulse discharge circuit 310. After a small propagation delay, the control circuit (not shown) creates a decoding signal DECODE that activates the appropriate subarray by connecting select line 460 to ground. When all three of the input signals to segment driver 450 are active, select line 460 is used to discharge the accumulated charge on the SOI transistors. This time, instead of discharging through segment driver 450 as shown in FIG. 4, the accumulated charge is dissipated through a pull-down transistor in inverter 624 which is located in pulse discharge circuit 310. This is accomplished as follows. In normal operation, to select a given memory subarray, the CTL signal for that subarray transitions from low to high. This CTL signal is also supplied to pulse discharge circuit 310 as an input signal. After a brief propagation delay through a delay element (invertors or other circuit device), circuit node 621 will transition from high to low. Circuit node 622 will generate a negative pulse and, after passing through an inverter, becomes a positive pulse at node 623. The positive signal or pulse applied to transistor 625 activates transistor 625 which, in turn, provides a path for discharging the word line drivers of memory circuit 500 through inverter 624. The pulse discharge signal generated by pulse generator 520 is the output signal from the pulse discharge circuit and, in a

preferred embodiment of the present invention, is supplied to the memory subarray just prior to the selection of the subarray for access. This means that the charge accumulated on the bodies of the SOI transistors has already been discharged when the request to access the subarray is received. By removing the charge before the first access occurs, the access time to the subarray is greatly enhanced. While it is possible to provide a discharge pulse prior to every access, this is not necessary. Once the initial accumulation of charge has been dissipated, as long as subsequent accesses are to the same subarray, there will not be very much charge accumulated in the subarray. By discharging the subarray prior to the first access only, the additional power requirements necessary to implement the invention are minimal. Once the control signal has selected a given segment. the control signal remains high and no transition of control signal is

Another preferred embodiment of the present invention utilizes selective connection of the body of SOI devices to reference ground which, as discussed above in reference to FIG. 7, will require some additional space on a typical chip. To use this method, the specific devices in a given circuit which are most critical to circuit access and performance time are identified and the bodies of those devices are connected to ground or V_{DD}. All other SOI devices in the circuit remain floating. For example, in FIG. 4, the body of transistor 432, and all other corresponding transistors in the other word line driver circuits, would be connected to ground. This method will successfully overcome most of the delays associated with the loading effect for circuit 400 during the first access cycle. However, because of the R/C delays described above, access to the top-most line driver in a memory circuit will still be much slower than for those line drivers located closest to the segment driver.

In summary, using a pulse body node discharge circuit can improve the access/switching time of SOI memory devices significantly. If the discharge pulse is only applied when first accessing a new subarray or segment, the extra power consumed will be negligible. In addition, the extra circuitry required to generate the pulse is negligible and can be added to a typical circuit layout without adversely impacting the overall chip size. If, on the other hand, the discharge pulse is applied to every memory access cycle, the access speed of the SOI memory device can be optimized. This implementation will cause some additional power consumption but remains desirable for those applications where high-speed memory access is necessary.

While the invention has been particularly shown and described with reference to preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the spirit and scope of the invention.

CLAIMS

1. In a circuit comprising a plurality of SOI devices wherein each of the plurality of SOI devices has a body, a mechanism for enhancing the performance of the circuit, the mechanism comprising:

a circuit component for discharging accumulated electrical potential from the body of the plurality of SOI devices.

2. The mechanism of claim 1 wherein the circuit component comprises a pulse discharge circuit.

3. The mechanism of claim 1 wherein the circuit component comprises a connection to ground for at least one of the bodies of the SOI devices.

4. The mechanism of claim 2 wherein the pulse discharge circuit comprises:

an input signal;

a delay element coupled to the input signal; and

an output signal coupled to the input signal, the output signal driving the circuit.

5. The mechanism of claim 2 wherein the pulse discharge circuit further comprises a pulse generator.

6. In a circuit comprising at least one SOI device, a method for enhancing the performance of the circuit, the method comprising the steps of:

providing a pulse discharge circuit connected to the at least one SOI device;

using the pulse discharge circuit to discharge any accumulated potential on the at least one SOI device prior to accessing the at least one SOI device.

7. The method of claim 6 wherein the circuit comprises a memory circuit.

8. The method of claim 6 wherein the pulse discharge circuit compises:

an input signal;

a delay element coupled to the input signal; and

an output signal coupled to the input signal, the output signal driving the circuit.

9. In a circuit comprising a plurality of SOI devices wherein each of the plurality of SOI devices has a body, a method for enhancing the performance of the circuit, the method comprising the step of:

selecting grounding the body of at least one of the plurality of SOI devices to dissipate electric potential.

10. The circuit of claim 9 wherein the plurality of SOI devices comprises a memory circuit.

11. In a circuit comprising a plurality of SOI devices wherein each of the plurality of SOI devices has a body, a method for enhancing the performance of the circuit, the method comprising the step of:

providing a pulse discharge circuit, the pulse discharge circuit having a pulse generator and the pulse generator being connected to the circuit;

using the pulse generator to generate a pulse;

discharging any accumulated potential on the body of at least one of the plurality of SOI devices by supplying the pulse from the pulse generator to the body of the at least one of the plurality of the SOI devices at a pre-determined time.

12. The method of claim 11 wherein the plurality of SOI devices comprises a memory circuit.

13. The method of claim 12 wherein the pre-determined time is just prior to accessing the memory circuit for reading or writing data.

*****

ABSTRACT OF THE DISCLOSURE

CIRCUIT AND METHODS TO IMPROVE THE OPERATION OF SOI DEVICES

According to the present invention, a circuit and methods for enhancing the operation of SOI fabricated devices are disclosed. In a preferred embodiment of the present invention, a pulse discharge circuit is provided. Here, a circuit is designed to provide a pulse that will discharge the accumulated electrical charge on the body of the SOI devices in the memory subarray just prior to the first access cycle. As explained above, once the accumulated charge has been dissipated, the speed penalty for successive accesses to the memory subarray is eliminated or greatly reduced. With a proper control signal, timing and sizing, this can be a very effective method to solve the problem associated with the SOI loading effect. Alternatively, instead of connecting the bodies of all SOI devices in a memory circuit to ground, the bodies of the N-channel FET pull-down devices of the local word line drivers can be selectively connected to a reference ground. This would enable the circuit to retain most of the speed advantages associated with SOI devices while overcoming the loading problem described above. With this preferred embodiment of the present invention, the major delay caused by the bipolar loading effect is minimized while the speed advantage due to providing a lower, variable Vt effect is preserved. The overall body resistance of the individual devices has a minimal effect on the device body potential.

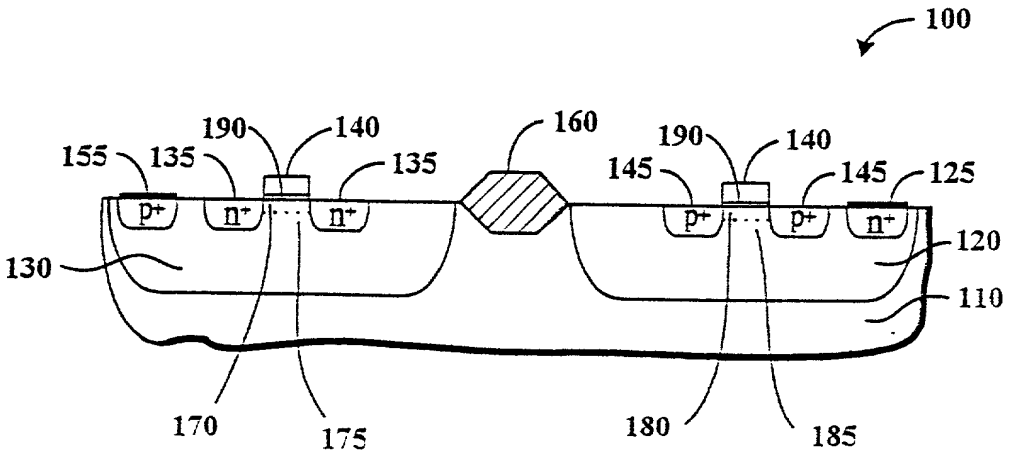
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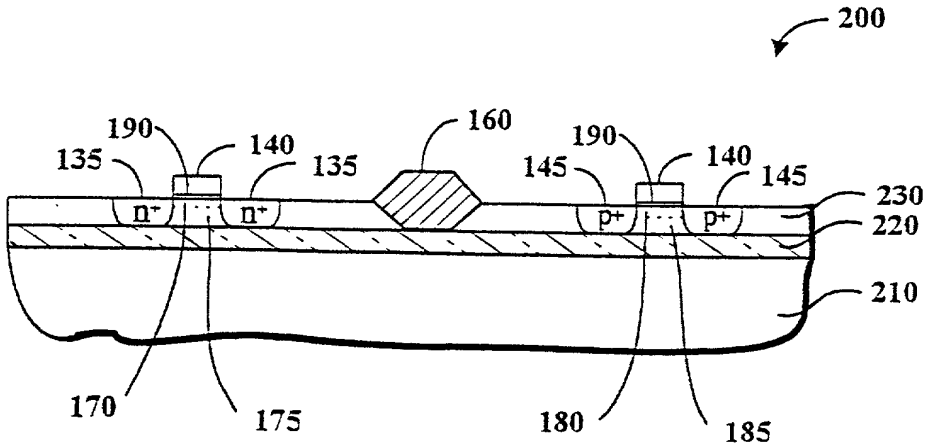
FIG. 1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160
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145
n+
n+
p+
p+
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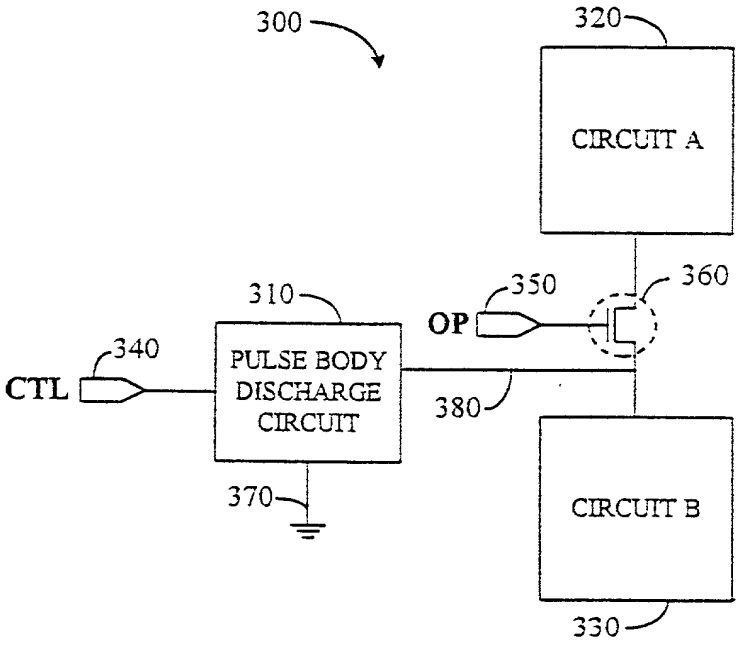
220
210
170
175
180
185

FIG. 2


300
320
CIRCUIT A
310
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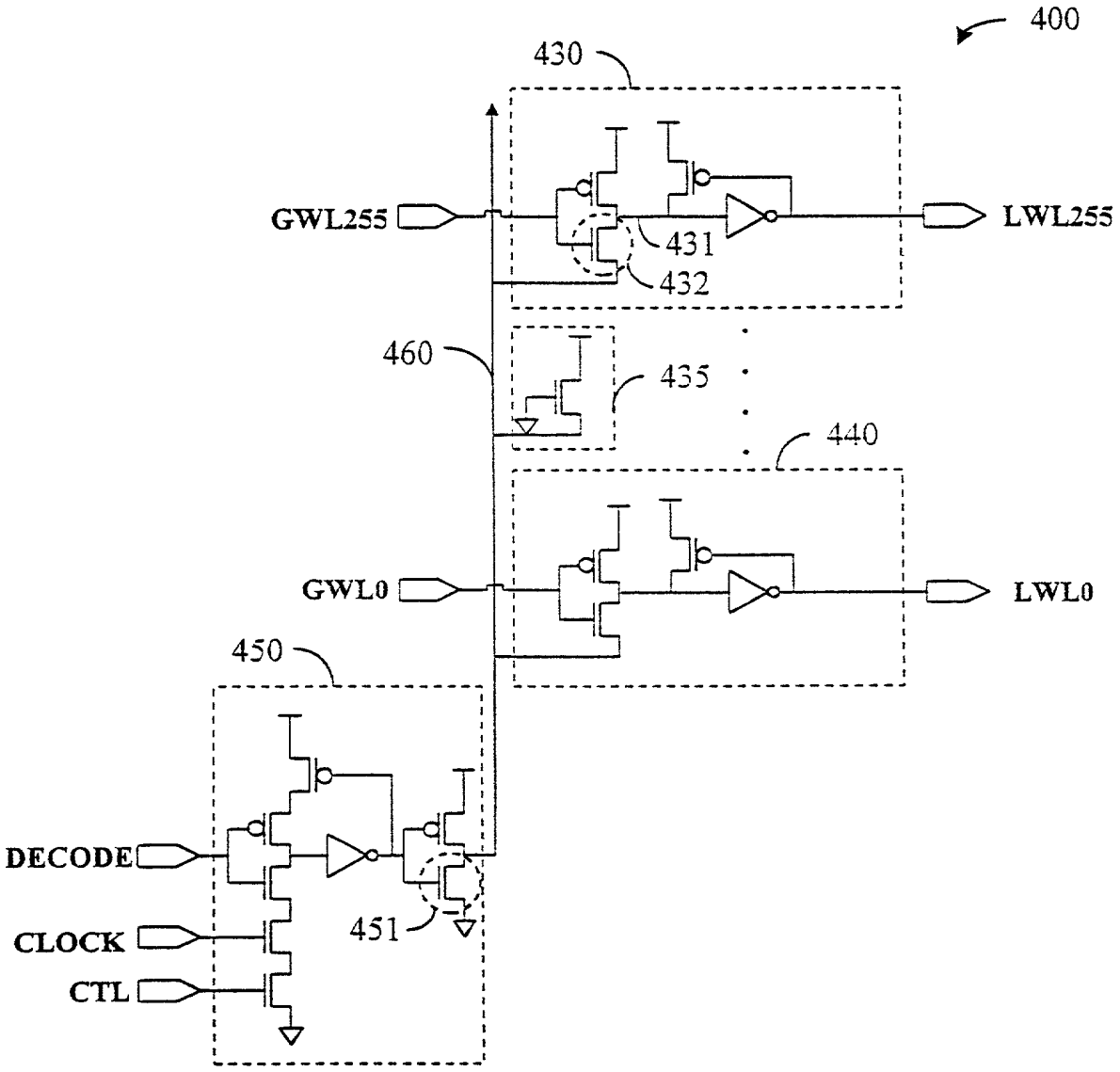
360
OP
340
CTL
PULSE BODY
DISCHARGE
CIRCUIT
380
370
CIRCUIT B
330

FIG. 3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LWL255
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432
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435
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GWL0
LWL0
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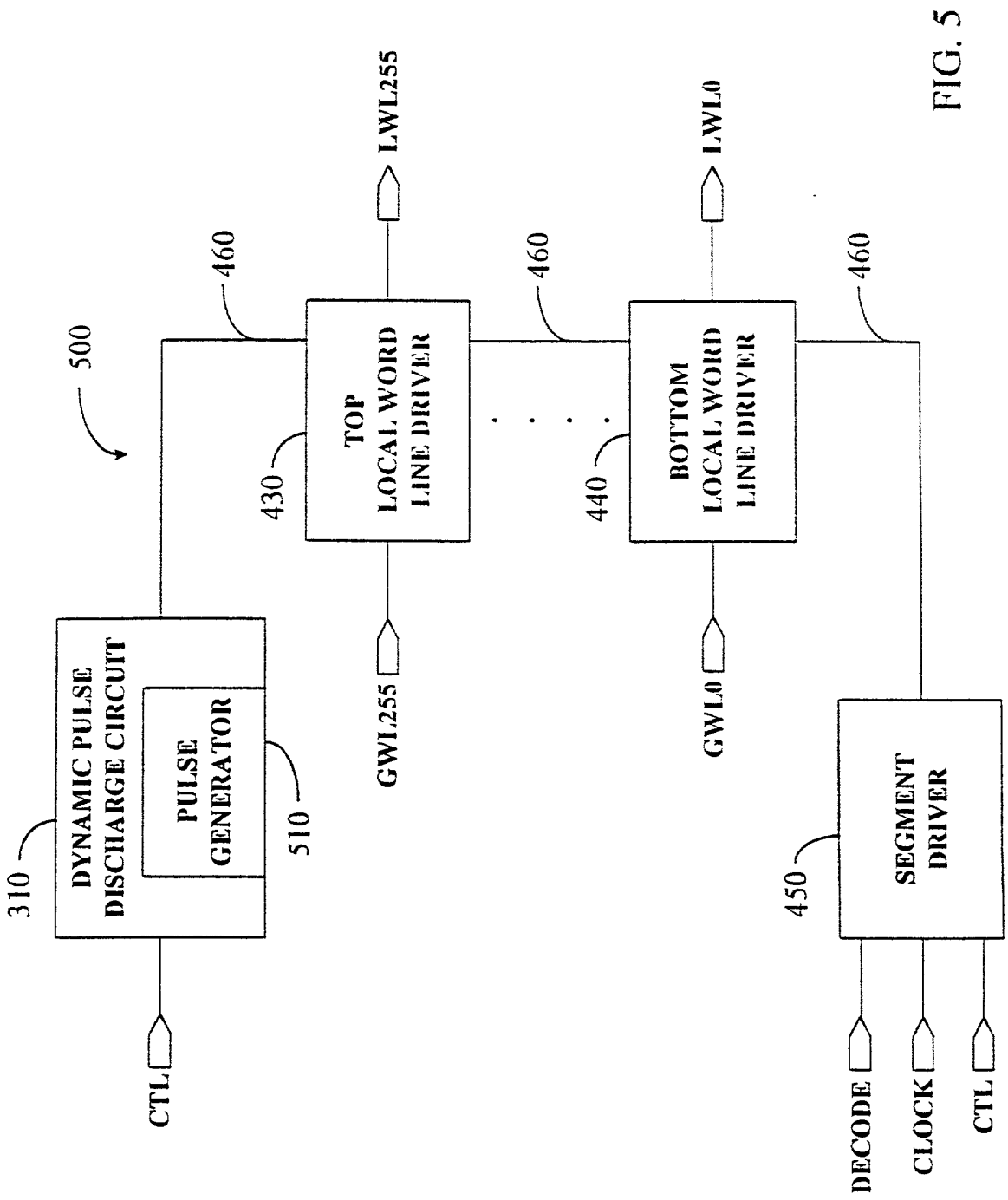
DECODE
CLOCK
CTL
451

FIG. 4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LWL255
LWL0
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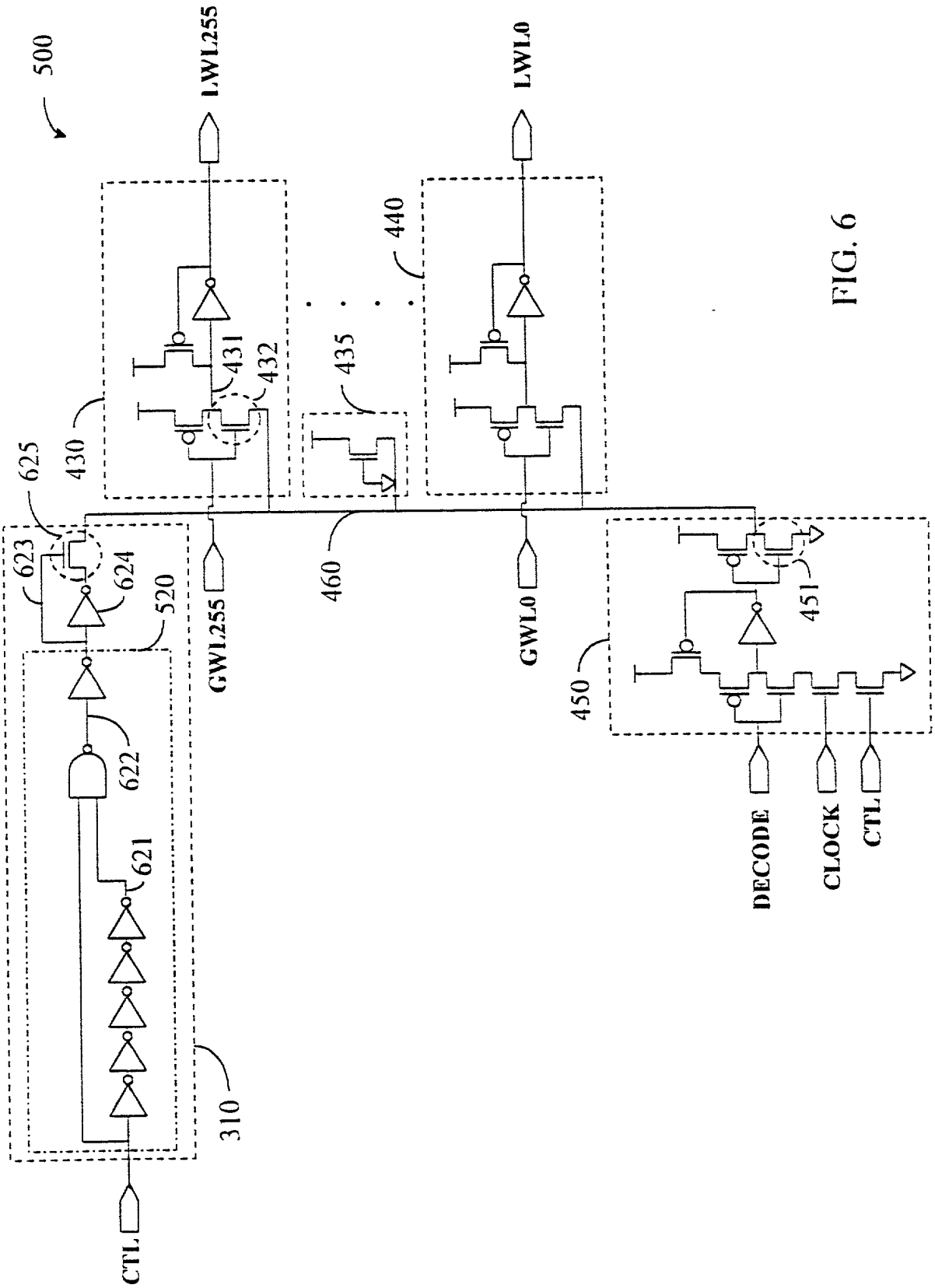
LOCAL WORD
LINE DRIVER
BOTTOM
LOCAL WORD
LINE DRIVER
430
440
DYNAMIC PULSE
DISCHARGE CIRCUIT
PULSE
GENERATOR
310
510
GWL255
GWL0
SEGMENT
DRIVER
450
CTL
DECODE
CLOCK
CTL

FIG. 5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LWL0
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432
435
440
625
623
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622
621
310
CTL
GWL255
460
GWL0
450
451
DECODE
CLOCK
CTL

FIG. 6

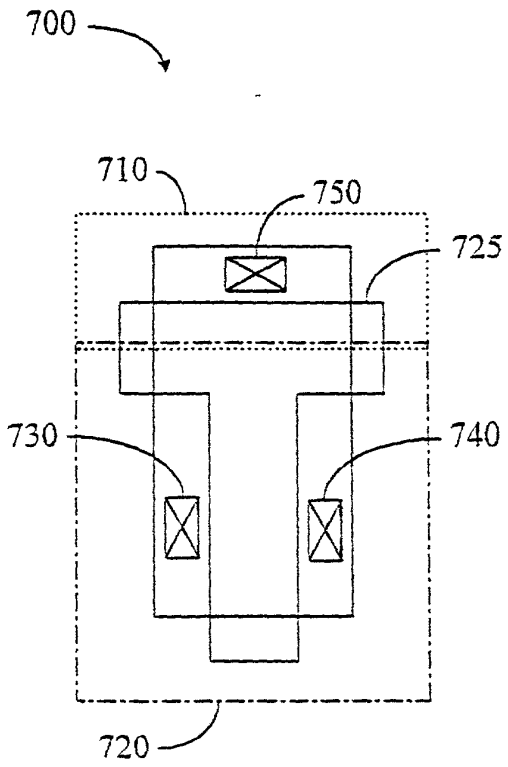

FIG. 7

DECLARATION FOR PATENT APPLICATION

As a below-named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

CIRCUIT AND METHODS TO IMPROVE THE OPERATION OF SOI DEVICES

the specification of which: (check one)

[XX] is attached hereto. [ ] was filed on _____ 19__, as United States Patent Application Serial No. or PCT International Application Number _____, and was amended on _____ 19__ (if applicable).

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			Priority Claimed
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60/044,251	April 23, 1997

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Send Correspondence and Direct Telephone Calls to:
George Vande Sande
(202) 331-7111

George Vande Sande
Pollock, Vande Sande & Priddy, R.L.L.P.
P.O. Box 19088
Washington, D.C. 20036-3425 U.S.A.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of sole or first inventor: Roy Childs Flaker (deceased) by Catherine O'Brien (heir)

Inventor's Signature X Catherine O'Brien Date X 4/9/98

Residence Address 2 Ridge Road, Essex Junction, Vermont 05452

Citizenship United States

Post Office Address Same as Above

[X] See next page for additional inventors

DECLARATION FOR PATENT APPLICATION

Page Two

Full name of second joint inventor (if any): Louis L. Hsu

Inventor's Signature _____ Date _____

Residence Address 7 Crosby Court, Fishkill, New York 12524

Citizenship United States

Post Office Address Same as Above

Full name of third joint inventor (if any): Jente B. Kuang

Inventor's Signature _____ Date _____

Residence Address 15 Four Winds Drive, Poughkeepsie, New York 12603

Citizenship Taiwan R.O.C.

Post Office Address Same as Above

Full name of fourth joint inventor (if any): _____

Inventor's Signature _____ Date _____

Residence Address _____

Citizenship _____

Post Office Address _____

Full name of fifth joint inventor (if any): _____

Inventor's Signature _____ Date _____

Residence Address _____

Citizenship _____

Post Office Address _____

Full name of sixth joint inventor (if any): _____

Inventor's Signature _____ Date _____

Residence Address _____

Citizenship _____

Post Office Address _____

Full name of seventh joint inventor (if any): _____

Inventor's Signature _____ Date _____

Residence Address _____

Citizenship _____

Post Office Address _____

Full name of eighth joint inventor (if any): _____

Inventor's Signature _____ Date _____

Residence Address _____

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Full name of sole or first inventor: Roy Childs Flaker (deceased) by Scott Flaker (heir)

Inventor's Signature X Scott Flaker Date X 3-31-99

Residence Address 2 Ridge Road, Essex Junction, Vermont 05452

Citizenship United States

Post Office Address Same as Above

[X] See next page for additional inventors

DECLARATION FOR PATENT APPLICATION

Page Two

Full name of second joint inventor (if any): Louis L. Hsu

Inventor's Signature _____ Date _____

Residence Address 7 Crosby Court, Fishkill, New York 12524

Citizenship United States

Post Office Address Same as Above

Full name of third joint inventor (if any): Jente B. Kuang

Inventor's Signature _____ Date _____

Residence Address 15 Four Winds Drive, Pouchkeepsie, New York 12603

Citizenship Taiwan R.O.C.

Post Office Address Same as Above

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Inventor's Signature _____ Date _____

Residence Address _____

Citizenship _____

Post Office Address _____

Full name of fifth joint inventor (if any): _____

Inventor's Signature _____ Date _____

Residence Address _____

Citizenship _____

Post Office Address _____

Full name of sixth joint inventor (if any): _____

Inventor's Signature _____ Date _____

Residence Address _____

Citizenship _____

Post Office Address _____

Full name of seventh joint inventor (if any): _____

Inventor's Signature _____ Date _____

Residence Address _____

Citizenship _____

Post Office Address _____

Full name of eighth joint inventor (if any): _____

Inventor's Signature _____ Date _____

Residence Address _____

Citizenship _____

Post Office Address _____

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Full name of sole or first inventor: Roy Childs Flaker (deceased) by Shirley A. Flaker (heir)

Inventor's Signature Shirley A. Flaker Date April 4, 1998

Residence Address 2 Ridge Road, Essex Junction, Vermont 05452

Citizenship United States

Post Office Address Same as Above

[X] See next page for additional inventors

DECLARATION FOR PATENT APPLICATION

Page Two

Full name of second joint inventor (if any): Louis L. Hsu
Inventor's Signature _____ Date _____
Residence Address 7 Crosby Court, Fishkill, New York 12524
Citizenship United States
Post Office Address Same as Above

Full name of third joint inventor (if any): Jente B. Kuang
Inventor's Signature _____ Date _____
Residence Address 15 Four Winds Drive, Poughkeepsie, New York 12603
Citizenship Taiwan R.O.C.
Post Office Address Same as Above

Full name of fourth joint inventor (if any): _____
Inventor's Signature _____ Date _____
Residence Address _____
Citizenship _____
Post Office Address _____

Full name of fifth joint inventor (if any): _____
Inventor's Signature _____ Date _____
Residence Address _____
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Full name of sixth joint inventor (if any): _____
Inventor's Signature _____ Date _____
Residence Address _____
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Post Office Address _____

Full name of seventh joint inventor (if any): _____
Inventor's Signature _____ Date _____
Residence Address _____
Citizenship _____
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Full name of eighth joint inventor (if any): _____
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Inventor's Signature: X Bruce Flaker Date: X 7/7/98

Residence Address 2 Ridge Road, Essex Junction, Vermont 05452

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Full name of eighth joint inventor (if any): _____

Inventor's Signature _____ Date _____

Residence Address _____

Citizenship _____

Post Office Address _____

DECLARATION FOR PATENT APPLICATION

As a below-named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

CIRCUIT AND METHODS TO IMPROVE THE OPERATION OF SOI DEVICES

the specification of which: (check one)

[XX] is attached hereto. [ ] was filed on _____ 19__, as United States Patent Application Serial No. or PCT International Application Number _____, and was amended on _____ 19__ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with 37 CFR § 1.56(a).

Prior Foreign Application(s): I hereby claim foreign priority benefits under 35 U.S.C. § 119(a)-(d) or §365(b) of any foreign application(s) for patent or inventor's certificate listed below, or § 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

(Application No.)	(Country)	(Day/Month/Year Filed)	Priority Claimed [ ] Yes [ ] No
(Application No.)	(Country)	(Day/Month/Year Filed)	[ ] Yes [ ] No
(Application No.)	(Country)	(Day/Month/Year Filed)	[ ] Yes [ ] No

I hereby claim the benefit under Title 35, United States Code § 119(e) of any United States provisional application(s) listed below:

Application No	Filing Date
60/044,251	April 23, 1997

I hereby claim the benefit under 35 U.S.C. § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by 35 U.S.C. § 112, first paragraph, I acknowledge the duty to disclose material information as defined in 37 CFR § 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(U.S. Application Serial No.)	(U.S. Filing Date)	(Status--patented, pending, abandoned)
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I hereby appoint the following attorneys and/or agents to prosecute this application and transact all business in the Patent and Trademark Office connected therewith: Joseph P. Abate, Reg. No. 30,382; Aziz M. Ahsan, Reg. No. 32,100; Ira D. Blecker, Reg. No. 29,894; Steven Capella, Reg. No. 33,086, Alison D. Mortinger, Reg. No. 39,306; Daryl K. Neff, Reg. No. 38,253; Eric W. Petraske, Reg. No. 28,459, H. Daniel Schnurmann, Reg. No. 35,791, Steven J. Soucar, Reg. No. 32,440, Marc D. Schechter, Reg. No. 28,989; all of INTERNATIONAL BUSINESS MACHINES CORPORATION; Elliott I. Pollock, Reg. No. 16,906, George Vande Sande, Reg. No. 17,276, Robert R. Priddy, Reg. No. 20,169, Burton A. Amernick, Reg. No. 24,852, Stanley B. Green, Reg. No. 24,351, Richard Wiener, Reg. No. 18,741, Townsend M. Belser, Jr., Reg. No. 22,956; Morris Liss, Reg. No. 24,510, Martin Abramson, Reg. No. 25,787, George R. Pettit, Reg. No. 27,369, Louis Woo, Reg. No. 31,730, Elzbieta Chlopecka, Reg. No. 32,767, Eric J. Franklin, Reg. No. 37,134 and Robert Scott Wales, Reg. No. 39,413; all of POLLOCK, VANDE SANDE & PRIDDY; John E. Hoel, Reg. No. 26,279, Christopher A. Hughes, Reg. No. 26,914, Edward A. Pennington, Reg. No. 32,588; Joseph C. Redmond, Jr., Reg. No. 18,753; all of MORGAN & FINNEGAN, L.L.P

Send Correspondence and Direct Telephone Calls to:
George Vande Sande
(202) 331-7111

George Vande Sande
Pollock, Vande Sande & Priddy, R.L.L.P.
P.O. Box 19088
Washington, D.C. 20036-3425 U.S.A.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of sole or first inventor: Roy Childs Flaker (deceased) by Anne Flaker (heir)

Inventor's Signature _____ Date 4/14/98

Residence Address 2 Ridge Road, Essex Junction, Vermont 05452

Citizenship United States

Post Office Address Same as Above

[X] See next page for additional inventors

DECLARATION FOR PATENT APPLICATION

Page Two

Full name of second joint inventor (if any): Louis L. Hsu

Inventor's Signature _____ Date _____

Residence Address 7 Crosby Court, Fishkill, New York 12524

Citizenship United States

Post Office Address Same as Above

Full name of third joint inventor (if any): Jente B. Kuang

Inventor's Signature _____ Date _____

Residence Address 15 Four Winds Drive, Pouchkeepsie, New York 12603

Citizenship Taiwan R.O.C.

Post Office Address Same as Above

Full name of fourth joint inventor (if any): _____

Inventor's Signature _____ Date _____

Residence Address _____

Citizenship _____

Post Office Address _____

Full name of fifth joint inventor (if any): _____

Inventor's Signature _____ Date _____

Residence Address _____

Citizenship _____

Post Office Address _____

Full name of sixth joint inventor (if any): _____

Inventor's Signature _____ Date _____

Residence Address _____

Citizenship _____

Post Office Address _____

Full name of seventh joint inventor (if any): _____

Inventor's Signature _____ Date _____

Residence Address _____

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Full name of sole or first inventor: Roy Childs Flaker (deceased) by Heather Flaker (heir)

Inventor's Signature X [signature] Date X 2/12/98

Residence Address 2 Ridge Road, Essex Junction, Vermont 05452

Citizenship United States

Post Office Address Same as Above

[X] See next page for additional inventors

DECLARATION FOR PATENT APPLICATION

Page Two

Full name of second joint inventor (if any): Louis L. Hsu

Inventor's Signature _____ Date _____

Residence Address 7 Crosby Court, Fishkill, New York 12524

Citizenship United States

Post Office Address Same as Above

Full name of third joint inventor (if any): Jente B. Kuang

Inventor's Signature _____ Date _____

Residence Address 15 Four Winds Drive, Poughkeepsie, New York 12603

Citizenship Taiwan R.O.C.

Post Office Address Same as Above

Full name of fourth joint inventor (if any): _____

Inventor's Signature _____ Date _____

Residence Address _____

Citizenship _____

Post Office Address _____

Full name of fifth joint inventor (if any): _____

Inventor's Signature _____ Date _____

Residence Address _____

Citizenship _____

Post Office Address _____

Full name of sixth joint inventor (if any): _____

Inventor's Signature _____ Date _____

Residence Address _____

Citizenship _____

Post Office Address _____

Full name of seventh joint inventor (if any): _____

Inventor's Signature _____ Date _____

Residence Address _____

Citizenship _____

Post Office Address _____

Full name of eighth joint inventor (if any): _____

Inventor's Signature _____ Date _____

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Full name of sole or first inventor: Roy Childs Flaker (deceased)

Inventor's Signature _____ Date _____

Residence Address 2 Ridge Road, Essex Junction, Vermont 05452

Citizenship United States

Post Office Address Same as Above

[X] See next page for additional inventors

DECLARATION FOR PATENT APPLICATION

Page Two

Full name of second joint inventor (if any): Louis L. Hsu
Inventor's Signature _____ Date 3/26/98
Residence Address 7 Crosby Court, Fishkill, New York 12524
Citizenship United States
Post Office Address Same as Above

Full name of third joint inventor (if any): Jente B. Kuang
Inventor's Signature _____ Date 4/8/1998
Residence Address 15 Four Winds Drive, Poughkeepsie, New York 12603
Citizenship Taiwan R.O.C.
Post Office Address Same as Above

Full name of fourth joint inventor (if any): _____
Inventor's Signature _____ Date _____
Residence Address _____
Citizenship _____
Post Office Address _____

Full name of fifth joint inventor (if any): _____
Inventor's Signature _____ Date _____
Residence Address _____
Citizenship _____
Post Office Address _____

Full name of sixth joint inventor (if any): _____
Inventor's Signature _____ Date _____
Residence Address _____
Citizenship _____
Post Office Address _____

Full name of seventh joint inventor (if any): _____
Inventor's Signature _____ Date _____
Residence Address _____
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